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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,235	11/18/2003	Yasushi Kubota	TI-35414	6910

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EXAMINER	
SHENG, TOM V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,235	KUBOTA ET AL.	
	Examiner	Art Unit	
	Tom V. Sheng	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-10,12 and 13* is/are rejected.

7)☒ Claim(s) *2-4 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 recites the limitation "the second direction" in line 21. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art, hereinafter APA, in view of Fujikawa (US 6,545,655 B1).

As for claim 1, APA teaches an integrated circuit for scan driving (fig. 9 and 10) being used in sequentially selecting and driving scanning lines (by using flip-flops SREG1-SREG176) in a display (display panel 102; fig. 5 and 7), which has said plural scanning lines and plural signal lines arranged crossing each other in a matrix configuration (page 2 paragraph 1), and which has a pixel arranged at each cross point (page 2 paragraph 1); in this integrated circuit for scan driving, comprising:

a chip (scan driver LSI 108), having plural output pads arranged as a column in a

first direction (see output pads/terminals OUT1-OUT176 arranged vertically as shown in fig. 8, 9 and 10; page 4 paragraph 2), plural drive circuits (DR1-DR176) for driving said scanning lines to the active state through said output pads, respectively (each DR drives a corresponding OUT as shown), and plural selection circuits (SREG1-SREG176) for individually selecting said driver circuits in a line-sequential scanning cycle (each SREG does select a corresponding driver circuit DR as shown). For details see page 4 paragraph 3 through page 6 paragraph 2.

However, the correspondence between the flip-flops SREG1-SREG176 and the drivers DR1-DR176 is not in order but crisscrossed instead. Consequently, APA does not teach the plural selection circuits SREG1-SREG176 in an order corresponding to the order of said scanning lines;

the odd-numbered output pads, driver circuits and selection circuits corresponding to odd-numbered scanning lines are all arranged in a first region,

the even-numbered output pads, driver circuits and selection circuits corresponding to the even-numbered scanning lines being all arranged in a second region adjacent to said first region in said first direction;

said first region, in an order corresponding to the order of said odd-numbered scanning lines, said odd-numbered output pads, driver circuits and selection circuits being arranged as columns in said first direction, respectively, and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines are arranged in the same row in the second direction nearly orthogonal to said first direction; and,

in said second region, in an order corresponding to the order of said even-numbered scanning lines, said even-numbered output pads, driver circuits and selection circuits are arranged as columns in said first direction, and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines being arranged in the same row in said second direction.

Fujikawa also teaches an integrated circuit for scan driving (vertical driver IC 33; fig. 6). Specifically, Fujikawa teaches two vertical drivers 25 and 26 formed adjacent to each other vertically in the vertical driver IC 33 (column 12 lines 41-53). Moreover, Fujikawa teaches that vertical driver 25 is for selecting pixels along odd-numbered rows and vertical driver 26 is for selecting pixels along even-numbered rows (column 13 lines 1-5). Further, the connections from the drivers 25 and 26 to the LCD panel 8A are clearly shown as crisscrossed in order to connect from odd outputs to odd rows and even outputs to even rows.

One of ordinary skill in the art would recognize by utilizing Fujikawa's teaching APA's correspondence between the selection circuits SREG1-SREG176 and drivers DR1-DR176 can be made in order and the odd-number circuits and even-numbered circuits can be separated into two regions. It is also clear that Fujikawa's way of combining two drivers into one IC saves chip space as the crisscrossing is now formed outside the IC (see fig. 6). Therefore, it would have been obvious to modify APA's scan driving IC in view of Fujikawa's teaching because of the space saving advantage.

As for claim 5, the direction in which the two drivers 25 and 26 are aligned is in the longitudinal direction of the scan driver IC 33. As shown in fig. 10 of APA, the output pads are clearly formed along one edge.

As for claim 6, it is inherent that there are input pads or terminals in order to receive inputs such as CPV and STV as shown in fig. 8 and 10 of APA.

As for claim 7, as shown in fig. 7, the scan driving IC 108 of APA is mounted on a TCP (page 2 paragraph 3).

5. Claims 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA and Fujikawa as applied to claim 1 above, and further in view of Wakai et al. (US 4,908,710), hereinafter Wakai.

Claim 8's first shift register, first drive section, second shift register, second drive section correspond to claim 1's odd-numbered selection circuits, odd-numbered driver circuits, even-numbered selection circuits, even-numbered driver circuits, respectively, and is rejected accordingly by rejection of claim 1. However, claim 8's limitation on "a second shift data shifted in phase by half a period of a second clock signal with respect to said first shift data corresponding to the second clock signal with its phase deviated by 180 from said first clock signal" is not recited in claim 1.

Both APA and Fujikawa teach using one vertical clock for driving the shift registers (CPV in the case of APA and VCK in the case of Fujikawa). Thus, APA and Fujikawa do not teach the above use of first and second clock signals. Wakai teaches using two clock signals (Φyo and Φye) to drive respective odd and even scanning

driving circuits (fig. 4-5; column 6 lines 17-46). Further, Wakai teaches that the two clock signals have inverse phase relation to each other (fig. 9; column 9 lines 30-32). One of ordinary skill in the art would recognize that Wakai's clock driving is a functionally equivalent alternative to modified APA's clock driving.

It would have been obvious to utilize Wakai's two clock signals driving in modified APA's scan driver IC, as both methods are functionally equivalent and would be selected based on design preference.

As for claims 9 and 12, Fujikawa's scan drivers 25 and 26 both have their register circuits and driver circuits aligned in the longitudinal axis of the IC.

As for claim 10, APA further teaches using decoders DEC1-DEC176 (fig. 9-10, part of driver circuits DR1-DR176) for controlling direction and initial stage as claimed.

As for claim 13, APA as modified by Fujikawa and Wakai has odd-numbered scan signals sequentially coming from a top driver and even-numbered scan signals sequentially coming from a bottom driver.

Allowable Subject Matter

6. Claims 2-4 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: none of the prior arts of record teaches, inter alia, the limitations

"the first transfer clock signal at a frequency half that of the line-sequential

scanning cycle" and "the second transfer clock signal at a frequency half that of the line-sequential scanning cycle and in a phase opposite to that of said first transfer clock signal" of claim 2,

"wherein said integrated circuit includes: a transfer clock generator that divides the fundamental clock signal that defines the cycle of line-sequential scanning in half, and a shift data generator that generates said first and second shift data in two consecutive cycles of said fundamental clock signal corresponding to the start pulse that indicates the timing of the start of a frame" of claim 4, and

"wherein said integrated circuit has a signal generator, to which the reference clock signal having a frequency double that of said first and second clock signals as well as a start pulse are input, and which generates said first and second clock signals and said first and second shift data on the base of said reference clock signal and said start pulse" of claim 11.

In other words, the use of two separate scan driving clocks that are in opposite phase to each other and both at twice the line scanning period are not taught or suggested in the prior arts.

Response to Arguments

8. Applicant's arguments filed on 10/3/2006 have been fully considered but they are not persuasive.

As for claims 1 and 5-7, Applicant argues that Fujikawa does not show the internal arrangement of the items within v-drivers 25, 26 which relate to the claim 1

requirements. The Examiner disagrees because Fujikawa does not need to show internal arrangements regarding the output pads, drive circuits and selection circuits because these elements are taught in the APA. Moreover, as analyzed in the rejection of claim 1, since the two vertical drivers 25 and 26 are distinctly separate and drive odd-numbered rows and even-numbered rows respectively, one of ordinary skill in the art would recognize that, by incorporating the teaching of Fujikawa, the selection circuits SREG1-SREG176 and the drivers DR1-DR176 can be made to correspond with each others in order and thus can be separated into two regions (top and bottom). This is advantageous as any crisscrossing can now be removed from within the integrated circuit, resulting in saving of chip space.

As for claims 8-10 and 12-13, Applicant argues that Wakai has shift registers 401 and 402 with clocks ϕyo and ϕye on opposite sides of the LCD panel; thus Wakai would not suggest anything about two shift registers and drivers on the same side. However, the teaching of the shift registers and drivers on the same side is already taught by the APA as modified by Fujikawa. The Examiner is only relying on the Wakai reference to teach the use of two separate clock signals ϕyo and ϕye to drive respective odd and even scanning driving circuits. Further the two clock signals have inverse phase relation to each other resulting in alternate output. Thus, the incorporation of Wakai's teaching of two separate clocks represents an functional equivalent alternative.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V. Sheng whose telephone number is (571) 272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tom Sheng

AMR A. AWAD
SUPERVISORY PATENT EXAMINER

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11/29/06

FIG. 1